DOCKET NO. 91-C-134D2 (STMI01-00098) **PATENT**
Customer No. 30425

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	:	Ravishankar Sundaresan
United States Serial No.	:	to be assigned
Filing Date	:	to be assigned
Prior United States Serial No.	:	08/193,725
Prior Filing Date	:	February 9, 1994
Prior Examiner	:	G.C. Eckert, II
Prior Group Art Unit	:	2815
Title	:	METHOD OF FORMING ASYMMETRICAL POLYSILICON THIN FILM TRANSISTOR (AS AMENDED)

MAIL STOP PATENT APPLICATION
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INFORMATION DISCLOSURE STATEMENT

Pursuant to the duty of disclosure under 37 C.F.R. § 1.56, Applicant submits this statement. This submittal is made in accordance with 37 C.F.R. §§ 1.97 and 1.98 and § 609 of the Manual of Patent Examining Procedure. The patents, publications and other information herein are listed below and on the attached Form PTO/SB/08. In accordance with 37 C.F.R.

§1.98(d), these references were previously cited by or submitted to, the Office in parent patent application Serial No. 08/193,725, and therefore copies of the cited references are not required.

U.S. Patent No.	Inventor	Date
4,581,623	Wang	Apr. 8, 1986
4,592,825	Yoshida	Aug. 28, 1990
5,112,764	Mitra et al	May 12, 1992
5,198,379	Adan	March 30, 1993
5,262,655	Ashida	Nov. 16, 1993

Foreign Patent No.	Country	Date
7132365	Japan	Aug. 16, 1982
3-260162	Japan	Oct. 27, 1988
1-179367	Japan	July 17, 1989
1-214172	Japan	Aug. 28, 1989
1-260857	Japan	Oct. 18, 1989
2-23669	Japan	Jan. 25, 1990
2-197173	Japan	Aug. 3, 1990
2-94478	Japan	April 5, 1990
0 457 434 A1	Europe	Nov. 21, 1991

Publications

OHKUBO, et al., "16Mbit SRAM Cell Technologies for 2.0V Operation," 1991 IEEE, IEDM, pp. 91-481 - 91-484.

LIU, et al., "Inverted Thin-Film Transistors with a Simple Self-Aligned Lightly Doped Drain Structure," IEEE Transactions on Electron Devices, Vol. 39, No. 12, December 1992.

LIU, et al., "High Reliability and High Performance 0.35μm Gate-Inverted TFT's for 16Mbit SRAM Applications Using Self-Aligned LDD Structures," 1992 IEEE, IEDM 92-823 - 92-826.

FURUTA, et al., "Hot-Carrier Induced Ion/Ioff Improvement of Offset PMOS TFT," 1991 Symposium on VLSI Technology, Digest of Technical Papers, IEEE Cat. No. 91, Ch. 3017-1, pp. 27-28.

WOLF, et al., Silicon Processing for the VLSI Era, Vol. 1 - Processing Technology, 1986, Lattice Press, pp. 308-309.

FICHTNER, W. et al., "Experimental Results on Submicron-Size p-Channel MOSFET's," IEEE Electron Device Letters, Vol. EDL-3, No. 2 (February 1982).

Article entitled "A Polysilicon Transistor Technology for Large Capacity SRAMs" by S. Ikeda, et al., IEDM 90, pp. 469-472, 1990.

Article entitled "A 5.9 μm^2 Super Low Power SRAM Cell Using a New Phase-Shift Lithography" by T. Yamanaka, et al., IEDM 90, pp. 477-480, 1990.

HAYASHI, et al., "A High Performance Polysilicon TFT Using RTA and Plasma Hydrogenation Application to High Stable SRAMs of 16Mbit and Beyond," 1992 Symposiun on VLSI Technology Digest of Technical Papers, 1992 IEEE, pp. 36-37.

Applicant hereby expressly reserves the right to swear behind the effective dates of any of the above Patents and to question the relevance and materiality of the Patents and Publications listed herein, in whole, in part, or in combination, subsequent to filing this Information Disclosure Statement.

Respectfully submitted,

DAVIS MUNCK, P.C.

Date: 3-29-04

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PTO/SB/08A (08-03)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 3

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	Ravishankar Sundaresan
Art Unit	
Examiner Name	
Attorney Docket Number	91-C-134D2 (STMI01-00098)

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	AA	US- 4,581,623	04/08/1986	Wang	
	AB	US- 4,592,825	08/28/1990	Yoshida	
	AC	US- 5,112,764	05/12/1992	Mitra et al	
	AD	US- 5,198,379	03/30/1993	Adan	
	AE	US- 5,262,655	11/16/1993	Ashida	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]
	AF	JP 7132365	08/16/1982			
	AG	JP 3-260162	10/27/1988	NEC Corp		
	AH	JP 1-179367	07/17/1989	NEC Corp		
	AI	JP 1-214172	08/28/1989	Nippon Teleg.		
	AJ	JP 1-260857	10/18/1989	Oki Electric		
	AK	JP 2-23669	01/25/1990	Seiko Epson		

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 2 of 3

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	Ravishankar Sundares
Art Unit	
Examiner Name	
Attorney Docket Number	91-C-134D2 (STMI01-0

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-			
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Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]
	BA	JP 2-197173	08/03/1990	Fujitsu Ltd.		
	BB	JP 2-99478	04/05/1990	Toshiba Corp.		
	BC	EP 0 457 434 A1	11/21/1991	Sharp Kabushiki		

Examiner Signature		Date Considered	

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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet	3	of	3

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	Ravishankar Sundares
Art Unit	
Examiner Name	
Attorney Docket Number	91-C-134D2 (STMI01-0

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	CA	OHKUBO, et al., "16Mbit SRAM Cell Technologies for 2.0V Operation," 1991 IEEE, IEDM, pp. 91-481 - 91-484.	
	CB	LIU, et al., "Inverted Thin-Film Transistors with a Simple Self-Aligned Lightly Doped Drain Structure," IEEE Transactions on Electron Devices, Vol. 39, No. 12, December 1992.	
	CC	LIU, et al., "High Reliability and High Performance 0.35μm Gate-Inverted TFT's for 16Mbit SRAM Applications Using Self-Aligned LDD Structures," 1992 IEEE, IEDM 92-823 - 92-826	
	CD	FURUTA, et al., "Hot-Carrier Induced Ion/Ioff Improvement of Offset PMOS TFT," 1991 Symposium on VLSI Technology, Digest of Technical Papers, IEEE Cat. No. 91, Ch. 3017-1, pp. 27-28	
	CE	FICHTNER, W. et al., "Experimental Results on Submicron-Size p-Channel MOSFET's," IEEE Electron Device Letters, Vol. EDL-3, No. 2 (February 1982).	
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	CH	HAYASHI, et al., "A High Performance Polysilicon TFT Using RTA and Plasma Hydrogenation Application to High Stable SRAMs of 16Mbit and Beyond," 1992 Symposium on VLSI Technology Digest of Technical Papers, 1992 IEEE, pp. 36-37	
	CI	WOLF, et al., Silicon Processing for the VLSI Era, Vol. 1 - Processing Technology, 1986, Lattice Press, pp. 308-309.	

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